NETWORK VARIABLE PRESERVING STEP-SIZE CONTROL IN WAVE DIGITAL FILTERS

Michael Jørgen Olsen[1], *Kurt James Werner*[2] *and François G. Germain*[1]

[1]Center for Computer Research in Music and Acoustics (CCRMA)
Stanford University
660 Lomita Drive, Stanford, CA 94305, USA
[mjolsen|francois]@ccrma.stanford.edu

[2]The Sonic Arts Research Centre (SARC)
School of Arts, English and Languages
Queen's University Belfast, UK
k.werner@qub.ac.uk

ABSTRACT

In this paper a new technique is introduced that allows for the variable step-size simulation of wave digital filters. The technique is based on the preservation of the underlying network variables which prevents fluctuation in the stored energy in reactive network elements when the step-size is changed. This method allows for the step-size variation of wave digital filters discretized with any passive discretization technique and works with both linear and nonlinear reference circuits. The usefulness of the technique with regards to audio circuit simulation is demonstrated via the case study of a relaxation oscillator where it is shown how the variable step-size technique can be used to mitigate frequency error that would otherwise occur with a fixed step-size simulation. Additionally, an example of how aliasing suppression techniques can be combined with physical modeling is given with an example of the polyBLEP antialiasing technique being applied to the output voltage signal of the relaxation oscillator.

1. INTRODUCTION

The physical modeling of analog reference systems is typically done using three main paradigms: wave digital filters (WDFs) [1–5], state space filters [6–8] and port-Hamiltonian [9] modeling. The WDF technique was developed in the 1970s with the digitization of classical ladder/lattice filters in mind. A need to retain the passivity of the original reference circuits was required so that the simulations would be stable under finite numeric conditions.

Since the early days of WDFs, the theory has evolved considerably in part due to interest from the physical modeling community in modeling historic audio circuits. The interest from this community has led to the development of new techniques that allow for the simulation of circuits containing complex topologies [4, 10, 11] and multiple/multiport nonlinearities [3, 12, 13]. There are also many interesting case studies of the simulation of reference circuits containing nonlinear network elements including distortion circuits containing diodes [14–16], tube amplifiers containing triodes [17–20] and circuits containing operational amplifiers (op amps) [14, 21].

The digital synthesis of classic analog waveforms and the antialiasing techniques needed to reduce their aliasing in the digital domain is another important thread of research. While there are a large number of techniques for synthesizing these signals, one of main methods involves bandlimiting the analog versions of the waveforms (or their derivatives) and either directly sampling the bandlimited version or forming approximate correction functions from it using polynomial interpolation [22–24]. A variant of the latter technique has also been applied to antialiasing in nonlinear waveshaping [25, 26]. Recently, a new antialiasing technique has been introduced in [26] and expanded upon in [27] that is based upon the differentiation of the antiderivatives of memoryless nonlinearities. The idea of combining physical modeling and antialiasing techniques has been suggested in [27].

To motivate the use of the variable step-size simulation method as well as provide an example of how physical modeling and antialiasing techniques can be combined, we study a square wave oscillator circuit commonly known as a relaxation oscillator. This circuit comes from a larger class of more complex oscillator circuits and was chosen to study due to its simplicity as well as two challenges that its simulation presents: significant frequency error which occurs when running the simulation with a fixed step-size and the need for an antialiasing method to suppress the aliasing present in the output waveform.

These two challenges are addressed as follows. First, the frequency error is reduced using the new variable step-size WDF simulation technique. Secondly, antialiasing of the output waveform is accomplished using the polyBLEP method [24] where domain knowledge of the circuit is used to estimate the exact location of the discontinuities in the output waveform.

In Section 2, a previous variable step-size WDF technique is reviewed and the new method is presented. The case study of the relaxation oscillator is given in Section 3. The circuit and its components are described in detail in Section 3.1. Section 3.2 explains how the WDF model of the circuit is derived and, in particular, how the op amp is implemented. The issues encountered when running the simulation with a fixed step-size are detailed in Section 3.3 and the way in which the new variable step-size technique is used to counter them is presented in Section 3.4. The technique in which polyBLEP is used to suppress output signal aliasing appears in Section 3.6 which is followed by the concluding thoughts in Section 4.

2. VARIABLE STEP-SIZE SIMULATION

Historically, WDFs were formulated to run at a fixed step-size using voltage waves [1] which are defined:

$$\begin{cases} a = \dfrac{1}{2}(v+i) \\ b = \dfrac{1}{2R}(v-i) \end{cases} \tag{1}$$

where a is called the "incident" wave, b is called the "reflected" wave and R is a free variable called the port resistance which is used to tune the system to eliminate delay free loops. A technique for simulating WDFs with a variable step-size was presented in [28] where it was shown that varying the step-size of an RLC circuit (Figure 1) discretized with the trapezoidal method led to an increase in energy in a zero-input simulation when it should have been passive. Their solution to the problem was to run the

Table 1: *Reactive Elements*

Element	Laplace Domain	Wave Domain	Port Resistance
capacitor	$v(s) = i(s)/(sC)$	$b[n] = a[n-1]$	$R = T/(2C)$
inductor	$v(s) = sLi(s)$	$b[n] = -a[n-1]$	$R = 2L/T$

variable step-size simulation on an equivalent circuit where the inductor was replaced with a network equivalent gyrator and capacitor pair. They stated that the equivalent circuit corresponded to discretization using the Gauss (midpoint) method and demonstrated that it exhibited the expected behavior of the reference circuit. Since their method depends on the replacement of inductors with network equivalent devices it is unclear whether the method will be guaranteed to work for all possible reference circuits.

In this section we introduce a new technique which allows WDFs discretized with any passive discretization technique, in particular the trapezoidal method, to be simulated with variable step-sizes. The development of the new technique was motivated by the fact that it was not obvious how the technique from [28] can be used with the relaxation oscillator circuit presented in the case study in Section 3. In Section 2.1, the general technique will be introduced and described. Later, in Section 3.4, it will be shown how varying the step-size fails to work with the example circuit and how the new technique can be used to mitigate the encountered issues.

2.1. Variable Step-Size WDF Simulation Technique

The variation of step-size in a WDF discretized with the trapezoidal rule (or other passive discretization technique) requires careful consideration due to the intricate relationship between the sampling rate and reactive network elements. Looking at the definition of wave variables (Equation (1)) and the port resistance values for reactive elements (Table 1) it is clear that the wave variables of these elements are directly coupled to the sampling rate.

The stored energy of a passive network is given by [28]:

$$\mathbf{w}_{k+1}^T \mathbf{G} \mathbf{w}_{k+1} - \mathbf{w}_k^T \mathbf{G} \mathbf{w}_k \leq \mathbf{x}_k^T \mathbf{G}_x \mathbf{x}_k, \tag{2}$$

where $\mathbf{w}_k$ is the vector of state values at time k, $\mathbf{G}$ is the diagonal matrix of the corresponding port conductances, $\mathbf{x}_k$ is the vector of source values and $\mathbf{G}_x$ is the diagonal matrix of source port conductances. In the case of zero input, Equation (2) implies that the stored energy will monotonically decrease towards zero. While Equation (2) is guaranteed to hold for passive networks under a fixed step-size, potential issues arise when one varies the step-size which changes the corresponding port resistances and the meaning of the stored energy.

Therefore, when changing the step-size it is not sufficient to just update the sampling rate, port resistances and matrices relating to the $\mathcal{R}$-type adaptor. It is also necessary (unless the technique from [28] can be used) to convert the wave variables to the representation that is consistent with the network variables and the new step-size before continuing the simulation.

The new step-size variation technique is based on maintaining the consistency of the network variables across step-size changes. Doing so ensures that the stored energy and the instantaneous power remain consistent as well. To do so, after changing the step-size and updating the port resistances, we then convert the stored energy by performing a wave variable transformation. Similar to the development of generalized C matrices in [29], the process is as

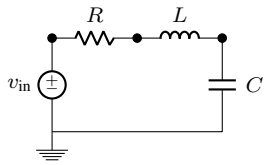


Figure 1: *RLC Circuit Schematic.*

follows to convert wave quantities a, b from sampling period T_k and port resistance R_k to new wave quantities $\hat{a}$, $\hat{b}$ with sampling period T_{k+1} and port resistance R_{k+1}. From the definition of voltage waves (Equation (1)), voltage and current are given in terms of the original wave quantities and port resistance by:

$$\begin{cases} v = \dfrac{a+b}{2} \\ i = \dfrac{a-b}{2R_k} \end{cases}$$

We then define the new wave quantities in terms of voltage, current and the new port resistance by:

$$\begin{cases} \hat{a} = v + R_{k+1} i \\ \hat{b} = v - R_{k+1} i \end{cases}$$

Combining these two sets of equations in matrix form yields the following conversion matrix:

$$\begin{bmatrix} \hat{a} \\ \hat{b} \end{bmatrix} = \frac{1}{2R_k} \begin{bmatrix} R_k + R_{k+1} & R_k - R_{k+1} \\ R_k - R_{k+1} & R_k + R_{k+1} \end{bmatrix} \begin{bmatrix} a \\ b \end{bmatrix} \tag{3}$$

In practice, however, $\hat{b}$ does not get used as the reflected waves of both inductors and capacitors only depend on $\hat{a}$. Through this transformation, both the power and the energy stored in the unit delays is preserved across step-sizes.

As a demonstration of the validity of this method, it was ran on the example RLC circuit used in [28] (Figure 1). The inductor incident waves from the simulation are shown in Figure 2 computed without correcting the wave quantities (as shown in the original paper), computed with our technique and also computed with a fixed step-size. As seen in the fixed step-size simulation trace, the traces should be exponentially decaying sinusoids. This correct behavior is seen in the trace of the simulation using the proposed technique. The trace is exponentially growing, however, when the wave quantities are not corrected.

To reiterate the process of correcting the wave variables, the following steps must be taken any time the sampling rate is altered:

1. Store the wave variables for all reactive elements and elements that appear above them in shared subtrees.
2. Readapt those network elements with the port resistance corresponding to the new sampling rate.
3. Convert the stored wave variables using the conversion matrix of Equation (3).
4. Update the relevant network elements with the converted wave variables.
5. If the structure contains an $\mathcal{R}$-type adaptor, update $\mathbf{S}$, $\mathbf{H}$, $\mathbf{E}$, $\mathbf{F}$, $\mathbf{M}$ and $\mathbf{N}$ using the updated port resistance values.
6. If wave quantities need to be output, convert them to a single unified representation (such as the one relating to audio rate).

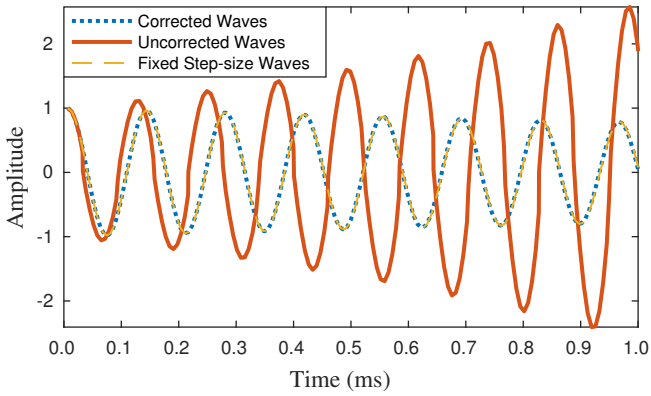


Figure 2: *Inductor incident waves from RLC circuit [28].*

3. RELAXATION OSCILLATOR CIRCUIT CASE STUDY

3.1. Circuit Description

The circuit to be modeled is called a relaxation oscillator [30] and is also known as an astable multivibrator circuit [31]. It contains the following components: a resistor R_1, a capacitor C_1, a voltage divider (R_2 and R_3) and an op amp. Throughout this paper it is assumed that $R_2 = R_3$ and that the op amp operates from rail-to-rail. The circuit schematic is shown in Figure 3.

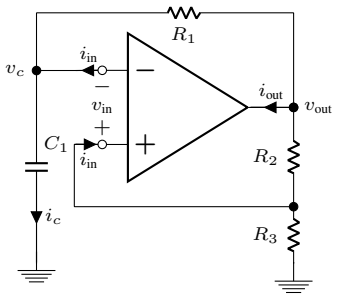


Figure 3: *Relaxation Oscillator Schematic.*

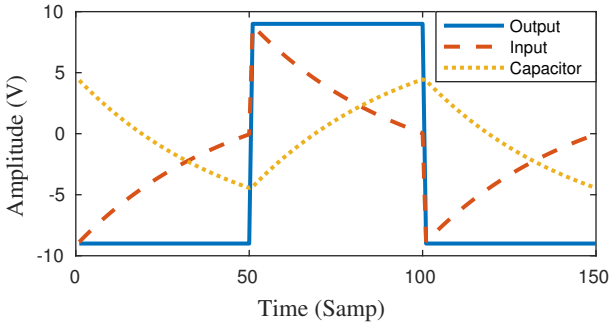


Figure 4: *Traces of the op amp input voltage, op amp output voltage and the capacitor voltage.*

The basic operation of the circuit is to behave as a comparator whose output swings high or low based on the whether the input voltage to the op amp is above or below a certain threshold value.

Table 2: *Relaxation Oscillator Circuit Component Values*

R_1	R_2	R_3	C_1	$V_{\max}$
10 kΩ	10 kΩ	10 kΩ	$1/(2\log(3)R_1F_0)$ F	9 V

The comparator is configured as a Schmitt trigger by means of the positive feedback path between v_{out} and i_{in}. Assuming that the op amp is powered with a rail voltage of $\pm V_{\max}$ and that it begins with the op amp in positive saturation, the capacitor begins charging towards $+V_{\max}$ with the time constant defined by R_1C_1. When the capacitor reaches $V_{\max}/2$, the op amp flips over to negative saturation and the capacitor begins discharging towards $-V_{\max}$. This behavior is illustrated in Figure 4 starting at sample number 50.

The period and frequency of oscillation are given by the following equations [31]:

$$\begin{cases} T_0 = 2\log(3)R_1C_1 \\ F_0 = 1/T_0 \end{cases} \tag{4}$$

The component values used during all simulations are given in Table 2. The capacitor value was used to control the frequency of oscillation and thus set based on the desired simulation frequency F_0 per Equation (4).

3.1.1. Op Amp Modeling

Operational amplifiers are very important devices in audio circuit design. Since, on the component level, op amps are composed of many passive electrical devices and potentially dozens of transistors, they are often modeled during design and simulation using simplified models. Depending on the level of detail needed, various techniques can be used to model op amps. More complicated linear "macromodels" are built up using linear one-ports (resistors, capacitors and dc sources) and two-ports (controlled sources) and can account for a variety of observed op amp behaviors. In the virtual analog context these models may be too complex when only one particular aspect of the model is needed. In the context of the relaxation oscillator the op amp behaves as a comparator. Based on the difference in voltage between the positive and negative terminals of v_{in} the op amp output goes into either positive or negative saturation.

A comparator may be represented ideally as a two-port nonlinear voltage-controlled voltage source (VCVS). This two-port device enforces two network constraints. The first is the nonlinear function $v_{\text{out}} = V_{\max}\,\text{sgn}(v_{\text{in}})$ and the second is the no input current criteria $i_{\text{in}} = 0$. We call v_{out}, i_{in} the dependent variables and v_{in}, i_{out} the independent variables and let

$$\boldsymbol{x}_C = [v_{\text{in}}\ i_{\text{out}}]^T \quad \text{and} \quad \boldsymbol{y}_C = [i_{\text{in}}\ v_{\text{out}}]^T. \tag{5}$$

From this we define the nonlinear relationship as

$$\boldsymbol{y}_C = f(\boldsymbol{x}_C) = \begin{bmatrix} 0 \\ V_{\max}\,\text{sgn}(v_{\text{in}}) \end{bmatrix}. \tag{6}$$

This particular comparator model was chosen to enforce an instantaneous transition between $\pm V_{\max}$ which exactly matches the step discontinuity which the polyBLEP method is designed to work with (see Section 3.6).

3.2. WDF Model of the Circuit

We form the WDF model using the techniques from [3, 4]. Either by visual inspection or via graph theoretic techniques, the schematic is rearranged as in Figure 5a so that all series and parallel subtrees are separated from the two-port nonlinearity by the remaining complex connections which are collectively called the $\mathcal{R}$-type adapter.

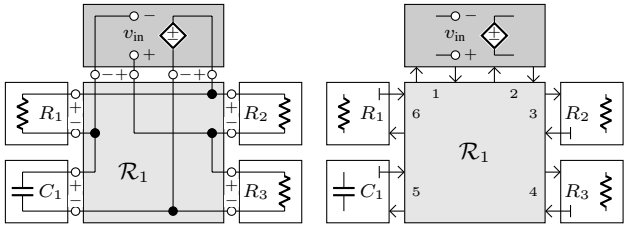
The techniques of [3] are used to determine the scattering behavior of the $\mathcal{R}$-type adaptor which is represented by the matrix $\mathbf{S}$. The following system of equations fully describes the relationship between the $\mathcal{R}$-type adaptor and the two-port nonlinearity:

$$\begin{cases} \boldsymbol{y}_C = f(\boldsymbol{x}_C) \\ \boldsymbol{x}_C = \mathbf{E}\boldsymbol{a}_E + \mathbf{F}\boldsymbol{y}_C \\ \boldsymbol{b}_E = \mathbf{M}\boldsymbol{a}_E + \mathbf{N}\boldsymbol{y}_C \end{cases} \quad \text{with} \quad \begin{aligned} \mathbf{E} &= \mathbf{C}_{12}(\mathbf{I} + \mathbf{S}_{11}\mathbf{H}\mathbf{C}_{22})\mathbf{S}_{12} \\ \mathbf{F} &= \mathbf{C}_{12}\mathbf{S}_{11}\mathbf{H}\mathbf{C}_{21} + \mathbf{C}_{11} \\ \mathbf{M} &= \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{22}\mathbf{S}_{12} + \mathbf{S}_{22} \\ \mathbf{N} &= \mathbf{S}_{21}\mathbf{H}\mathbf{C}_{21} \end{aligned} \tag{7}$$

where

$$\mathbf{S} = \begin{bmatrix} \mathbf{S}_{11} & \mathbf{S}_{12} \\ \mathbf{S}_{21} & \mathbf{S}_{22} \end{bmatrix}, \qquad \mathbf{H} = (\mathbf{I} - \mathbf{C}_{22}\mathbf{S}_{11})^{-1}$$

and $\boldsymbol{a}_E = [a_3\, a_4\, a_5\, a_6]$ is the vector of incident waves from the $\mathcal{R}$-type adaptor.



(a) *Schematic Rearranged.* (b) *WDF.*

Figure 5: *Relaxation Oscillator Rearranged Schematic and WDF.*

As discussed in Section 3.1.1, the input variables, output variables and comparator model of the op amp are given by Equations (5) and (6). We then use the definition of voltage waves (Equation (1)) and the signal flow relationship of the nonlinear device quantities:

$$\begin{bmatrix} \boldsymbol{x}_C \\ \boldsymbol{b} \end{bmatrix} = \mathbf{C} \begin{bmatrix} \boldsymbol{y}_C \\ \boldsymbol{a} \end{bmatrix}$$

where

$$\boldsymbol{b} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \quad \text{and} \quad \boldsymbol{a} = \begin{bmatrix} a_1 \\ a_2 \end{bmatrix},$$

to determine the generalized conversion matrix $\mathbf{C}$ [29]:

$$\mathbf{C} = \begin{bmatrix} \mathbf{C}_{11} & \mathbf{C}_{12} \\ \mathbf{C}_{21} & \mathbf{C}_{22} \end{bmatrix} = \left[\begin{array}{cc|cc} -R_1 & 0 & 1 & 0 \\ 0 & -G_2 & 0 & G_2 \\ \hline -2R_1 & 0 & 1 & 0 \\ 0 & 2 & 0 & -1 \end{array}\right]$$

where R_1 and G_2 refer to the port resistance and port conductance of ports 1 and 2, respectively.

3.2.1. Numerical Solution of the Nonlinearity

In [5] it was shown how, in general, nonlinearities can be solved using iterative techniques. In the case of this particular circuit, however, the nonlinear relationship is modeled as a step discontinuity for which iterative techniques struggle to converge quickly if at all. Through inspection of the WDF equations representing the nonlinearity it was found that they are formed in such a way that a quasi-analytic solution can be determined.

From Equation (7), we get the following complete description of the nonlinear system of equations to be solved:

$$\boldsymbol{x}_C = \mathbf{E}\boldsymbol{a}_E + \mathbf{F}f(\boldsymbol{x}_C) \tag{8}$$

where, for this particular circuit, $\mathbf{E}$ is a 2×4 matrix and $\mathbf{F}$ is a 2×2 matrix. We use domain knowledge of the circuit to simplify the nonlinear system of equations. Since a_3, a_4 and a_6 are the incident waves relating to the resistors, which are always zero, and since i_{in} is also zero, the following simplified expression is obtained:

$$\begin{bmatrix} v_{\text{in}} \\ i_{\text{out}} \end{bmatrix} = \begin{bmatrix} e_{13}a_5 + f_{12}V_{\max}\,\text{sgn}(v_{\text{in}}) \\ e_{23}a_5 + f_{22}V_{\max}\,\text{sgn}(v_{\text{in}}) \end{bmatrix}.$$

The values of v_{out} and i_{out} are dependent on the value and sign of v_{in} and the constant values from the $\mathbf{E}$ and $\mathbf{F}$ matrices. Therefore, the nonlinearity can be solved algorithmically using the following pseudocode:

Algorithm 1: Nonlinearity Solver

```
1  if n − 1 < 1
2    initialize sgn_vin to ±1
3  else
4    sgn_vin ← sgn(v_in[n − 1])
5  end if
6
7  v_in[n] ← e13 a5[n] + f12 V_max · sgn_vin
8  x_C ← E a_E[n] + F · [0  V_max sgn(v_in[n])]^T
9
10 if E a_E[n] + F · [0  V_max sgn_vin]^T − x_C ≠ 0
11   sgn_vin ← −sgn_vin
12   v_in[n] ← e13 a5[n] + f12 V_max · sgn_vin
13   x_C ← E a_E[n] + F · [0  V_max sgn(v_in[n])]^T
14 end if
15
16 y_C ← [0  V_max sgn(v_in[n])]^T
17 return x_C, y_C
```

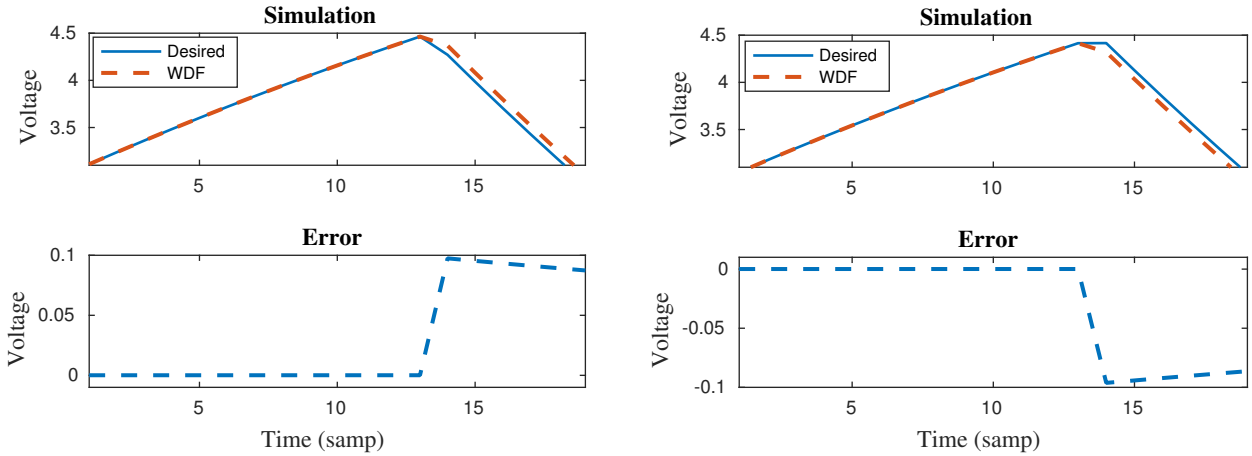
The algorithm determines the correct values for v_{in} and v_{out} by guessing the sign of v_{in} (using the sign of the previous value of v_{in}) and checking whether or not the result is consistent with Equation (8). If it is consistent, then that is the correct value of v_{in} and it can be used to calculate $\boldsymbol{x}_C$ and $\boldsymbol{y}_C$. Otherwise, the sign is flipped and then the only other possible solution is calculated.

3.3. Problems Resulting from the Fixed Step-size Simulation

3.3.1. Simulation Error

By running the simulation with a fixed step-size at a variety of frequencies and then analyzing the spectrum of the output voltage of the op amp it was determined that a noticeable amount of frequency error was occurring in the simulation. Upon more detailed analysis of the circuit output, it was determined that the majority of the error was occurring around the location of the discontinuities in the component voltages.

As shown in Figure 6, there are two related error scenarios. In the first, as seen in Figure 6a, it is possible that the error leads to the simulation running at a lower frequency than desired due to an overshoot at the first transition of the capacitor voltage. In the second scenario, Figure 6b, the opposite situation occurs and



(a) *Capacitor voltage error when simulation frequency is less than the desired frequency.*

(b) *Capacitor voltage error when simulation frequency is greater than the desired frequency.*

Figure 6: *Capacitor voltage error scenarios.*

the simulation runs at a higher frequency than desired. In both Figure 4 and Figure 6, the simulation was run at 44.1 kHz sampling rate with a desired period of 101 samples with the average period of the simulations being 102 and 100 for Figures 6a and 6b, respectively.

3.3.2. Simulation Frequency

It was determined experimentally that the overshoot/undershoot error identified in Section 3.3.1 causes the fundamental period T_0 of the simulation to become "phase-locked" to an even integer length period. In the lucky case that T_0 was an even integer, it was found that the fundamental period of simulation $\widehat{T}_0$ was equal to T_0 and so the simulation did not contain any frequency error. For any other choice of T_0, however, two possible values of $\widehat{T}_0$ were observed:

$$\widehat{T}_0^+ = \text{floor}(T_0) - (\text{floor}(T_0) \bmod 2) \tag{9a}$$

$$\widehat{T}_0^- = \text{ceil}(T_0) + (\text{ceil}(T_0) \bmod 2) \tag{9b}$$

The phase-locking of the frequency that occurred from these errors occurred immediately such that $\widehat{T}_0$ was the observed period of oscillation for every period of the simulation beginning with the first complete period.

Since it is not possible to derive an analytic expression for the actual simulation frequency error, we derive an expression for the worst case error in order to investigate the general behavior of the maximum possible frequency error. The worst case frequency error curve in cents can be derived using the following formula:

$$\Delta F_{\text{max}} = 1200 \max\left(\left|\log_2\left(\frac{\hat{F}_0^-}{F_0}\right)\right|, \left|\log_2\left(\frac{\hat{F}_0^+}{F_0}\right)\right|\right) \tag{10}$$

where

$$\begin{cases} \widehat{F}_0^+ = F_s/\widehat{T}_0^+ \\ \widehat{F}_0^- = F_s/\widehat{T}_0^- \end{cases}$$

where F_s is the sampling rate. Equation (10) gives the worst case frequency error estimation as determined by the largest possible rounding error occurring in the simulation period.

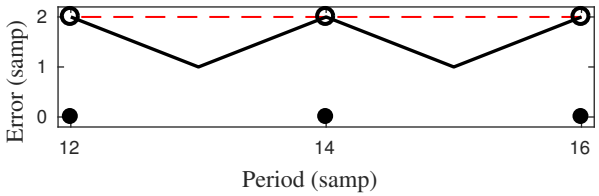
A portion of the resulting curve is shown in Figure 7a. The minimum points on the curve corresponding to an error of one sample occur at odd integer periods which are equal distance from the nearest even integer periods. From those points, the error curve increases in either direction approaching a theoretical limit of two samples (indicated by open circles). Finally, at the even integer period values, there is no error in the period which is notated by the solid black dots. The dotted red line shows the maximum error limit which was used in the computation of the frequency error curves shown in Figure 7b.

Hypothetically assuming that a frequency error of six cents is imperceptible at all frequencies, the worst case error curves (Figure 7b) given an idea of the level of oversampling necessary for the fixed step-size simulation error to fall below that level. It is also evident that the maximum possible simulation error is frequency dependent and clearly increasing with frequency. Thus, the amount of oversampling necessary to mitigate the worst case error is coupled to the desired frequency of simulation.

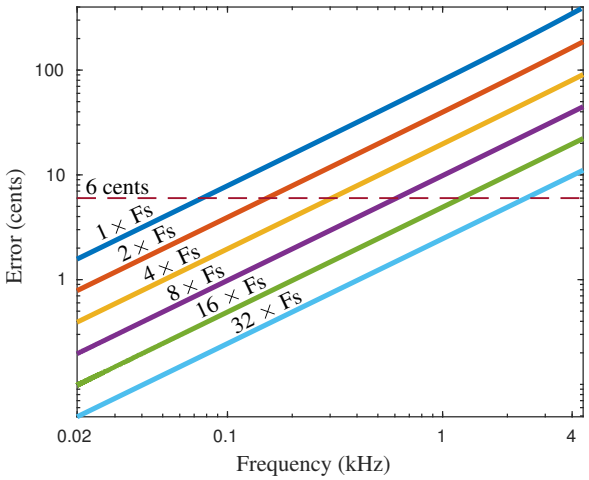
3.4. Variable Step-size Simulation of the Oscillator WDF

Variable step-size ODE solvers typically utilize an automatic step-size selection algorithm [28, 32]. The step-size is determined by estimating the amount of simulation error that would result from continuing to use the current step-size and then either increasing or decreasing the step-size based on the result of that error calculation.

Since the majority of the simulation error in the fixed step-size simulation of the relaxation oscillator occurs in the region of the discontinuities in the simulation voltages and the accuracy of the simulation frequency is coupled to the amount of oversampling performed, it would be highly desirable to limit oversampling to just those regions and to also have control over the rate of oversampling. This would have the benefit of reducing the computational cost as compared to just oversampling the simulation with a



(a) *Local Maximum Possible Period Error in Samples.*



(b) *Maximum Frequency Error in Cents for Different Levels of Upsampling.*

Figure 7: *Worst Case Period and Frequency Error.*

fixed step-size and would allow the user to control the amount of maximum possible frequency error in the simulation. To accomplish this, domain knowledge of the circuit is used to predict the occurrence of discontinuities and oversampling is performed only in that region.

3.4.1. Detection of Discontinuity Regions

As seen in Figure 4, the step discontinuities in the op amp output voltage occur whenever the op amp input voltage crosses zero which also corresponds to the point where the capacitor changes state. Thus, we use the input voltage and an extrapolation formula based on its theoretical behavior to predict the occurrences of zero-crossings and, therefore, of the step discontinuities.

This is done using the following extrapolation formula:

$$\hat{v}_{\text{in}}[n+1] = -\left(\frac{\text{sgn}(v_{\text{in}}[n])V_{\text{max}}}{2} + v_{\text{in}}[n]\right)\left(1 - e^{\frac{-T}{R_1 C_1}}\right) + v_{\text{in}}[n], \quad (11)$$

where v_{in} is the input voltage of the op amp and sgn is the signum function.

The formula represents the theoretical charge and discharge exhibited in the input voltage of the op amp. Therefore, the detection of the discontinuities is expected to be highly accurate so that the simulation can be ran at the higher sampling rate for a limited number of samples.

3.4.2. Extrapolation and Variable Step-size Algorithm

Algorithm 2 gives pseudocode for the extrapolation and step-size modification routine used in the simulation. The algorithm detects if a zero-crossing will happen in the op amp input voltage during the next two future samples. If so, the system is updated to the higher sampling rate and runs the equivalent of three original rate samples at the higher rate. Only the higher rate samples corresponding to lower rate samples are stored (with wave quantities converted to the lower rate representation) so that the output of the simulation always corresponds to the base sampling rate. Finally, the system returns to running at the original sampling rate until the next discontinuity is detected. It is enforced that the higher sampling rate is an integer multiple of the base sampling rate so that interpolation can be avoided during decimation.

Algorithm 2: Extrapolation/Step-Size Algorithm

```
1  vin_nm1 ← v_in[n − 1]
2  extrapolate vin_n from vin_nm1 using Equation (11)
3  extrapolate vin_np1 from vin_n using Equation (11)
4  if vin_n · vin_np1 ≤ 0:
5    nSamps = 3
6    K ← the oversampling factor
7    k ← nSamps · K
8    Update system to new sampling rate
9    for i = 1 : k
10     iterate system 1 sample
11     if i mod K = 0
12       save system values as (n + i/K − 1)-th values
13       convert saved wave quantities using Eq. (3)
14     end if
15   Update system back to original sampling rate
16 end if
```

It should be noted that anti-aliasing is not performed at the decimation stage. This is because the anti-alias filtering of v_{out} will change the dynamics of the system, through modification of the output voltage, affecting the energy stored in the capacitor therefore affecting the frequency of oscillation. In order for the simulation frequency to be as accurate as possible, which corresponds to the simulation error being as small as possible, we allow the aliasing to occur within the simulation. How to suppress the aliasing inherent in the output voltage is the subject of Section 3.6.

3.5. Variable Step-size Method with the Relaxation Oscillator Simulation

In Section 2, a new technique was introduced for the variable step-size simulation of a WDF. The need for the technique arose from the fact that the relaxation oscillator is a nonlinear circuit and also does not contain any inductors. Therefore, it was unclear how the technique from [28] could be implemented with this particular circuit. If the Gauss method is equivalent to the trapezoidal rule for any circuit that does not contain inductors, then variable step-size simulation without using the technique presented in Section 2 will lead to large fluctuations in the energy stored in the delay registers of the capacitor.

This can be clearly seen in Figure 8 which shows the incident waves and stored energy of the capacitor from three different simulations. The desired fundamental period of the simulation was 100.25 samples so that a fixed step-size simulation run at $8\times$ oversampling would yield an output waveform with no frequency error. The corrected and uncorrected traces show the incident waves of the capacitor when trapezoidal discretization is used with and without the technique proposed in Section 2. The figure shows that large fluctuations in stored energy occur when the step-size

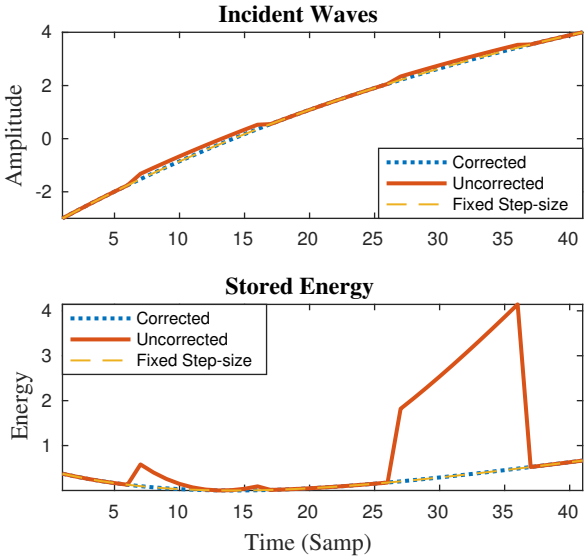


Figure 8: *Incident waves and the stored energy in the capacitor for the relaxation oscillator circuit run with a fixed step-size and different variable step-size methods.*

is changed without using the new technique. Conversely, when the new technique is used, the incident waves and energy perfectly match the corresponding traces from the fixed step-size simulation.

3.6. Aliasing Suppression in the Output Signal

Due to the use of the ideal comparator VCVS characteristic to model the op amp behavior, the output voltage of the op amp is a square wave that instantaneously switches between $\pm V_{\max}$. Thus, the presence of step discontinuities in the output waveform results in a similar amount of aliasing as arises from trivial synthesis of a square waveform. To minimize the aliasing, we use the polyBLEP [24] antialiasing technique.

In the original method, the square wave is generated using a phase accumulator which allows for an exact calculation of the location of the discontinuities. This fractional delay value is then used to determine the exact placement of samples of the polyBLEP residual function which are added to one or more samples of the output waveform before and after each discontinuity.

The WDF simulation of the example circuit in this paper does not lend itself to a simple determination of the phase of the op amp output voltage. We use a method based on the extrapolation technique developed in Section 3.4.1 for determining the fractional delay of the occurrence of each discontinuity. During the higher rate processing, after the polarity of the input voltage has flipped, a version of Equation (11) is used to determine the fractional delay in terms of the higher sampling rate:

$$dx_K = 1 + R_1 C_1 K F_s \log\left(\frac{\operatorname{sgn}(v_{in}[i-1])V_{\max}}{\operatorname{sgn}(v_{in}[i-1])V_{\max} + 2v_{in}[i-1]}\right).$$

From this, the fractional delay is expressed in terms of the original sampling rate by adding the distance to the next lower rate sample:

$$d = \frac{(K-i) \bmod K}{K}$$

to the appropriately scaled fractional delay value:

$$dx = \frac{dx_K}{K} + d$$

where i and K are as defined in Algorithm 2.

Depending on the chosen polyBLEP method, a number of v_{out} samples before and after the step discontinuity have to be altered to include the polyBLEP residual amount for the chosen scheme. This is done exactly the same way as in the original paper.

Due to the effect that the polyBLEP residual has on the dynamics of the simulations, the polyBLEP residual is applied to a separate output signal path so that it does not affect the internal dynamics of the simulation. Thus, the modified output voltage is not fed back through the feedback path of the circuit.

Third-order Lagrange polynomial polyBLEP residual functions were used to reduce the aliasing for a simulation run with a fundamental frequency of 100π at a sampling rate of 44.1 kHz with a higher rate of $16 \times F_s$ for a frequency error of $9.7\text{e}{-4}$ cents. The result of applying the polyBLEP residual function to the output voltage is shown in Figure 9 where the upper image shows the spectrum of the original output voltage and the lower image shows the spectrum of the output voltage with the polyBLEP residual applied. Clearly, the aliasing in the spectrum of the output voltage with polyBLEP residuals applied is falling off at a much steeper rate than the original waveform's spectrum. It is also evident that the amplitude of the higher harmonics in the spectrum of the alias suppressed waveform are falling off more quickly than the theoretical amplitudes. This can be fixed using a high shelf equalization filter. Example filter coefficients are given in [24].

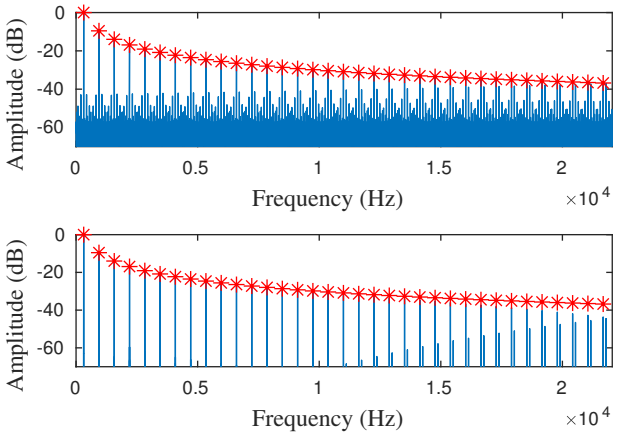


Figure 9: *Spectrums of the output voltages of a simulation run without polyBLEP (top) and with (bottom). The theoretical amplitude of the harmonics are indicated by asterisks.*

4. CONCLUSION

In this paper a new technique was introduced for the variable step-size simulation of wave digital filters. A conversion of the wave variable quantities of reactive network elements is performed any time that the sampling rate is changed. Our method is novel in that it ensures that the network variables are preserved which enforces that the energy stored in the reactive elements is preserved as well.

In [28], the variable step-size simulation of WDFs discretized with the trapezoidal rule was identified as an open problem. By identifying the relationship between wave variables and network variables it has been shown how the correct behavior can achieved in a WDF model which directly discretizes the reactive elements and does not use network component equivalencies. The validity of the technique holds regardless of the discretization technique being used to discretize the reactive network elements. With WDFs, however, it is well known that passive discretization techniques must be used.

Through the case study of a relaxation oscillator circuit, the need for the new variable step-size technique was demonstrated. The variable step-size WDF simulation technique was used to mitigate frequency error related to the discontinuities in the device voltages. An extrapolation formula was used to estimate the occurrence of future zero crossings in the input voltage of the op amp. This allowed the system to be switched to the higher simulation rate for a short duration of three base rate samples encompassing the occurrence of the step discontinuity in the op amp output voltage. It was also demonstrated how physical modeling and antialiasing techniques can be combined to yield an accurate and alias-reduced simulation of the relaxation oscillator circuit. The polyBLEP antialiasing technique was used and the oversampling from the variable step-size technique had the additional benefit of improving the estimate of the fractional delay thus further improving the accuracy of the polyBLEP method.

5. REFERENCES

[1] A. Fettweis, "Wave digital filters: Theory and practice," *Proc. IEEE*, vol. 74, no. 2, pp. 270–327, Feb. 1986.

[2] G. De Sanctis and A. Sarti, "Virtual analog modeling in the wave-digital domain," *IEEE Trans. Audio, Speech, Language Process.*, vol. 18, no. 4, pp. 715–727, May 2010.

[3] K. J. Werner, V. Nangia, J. O. Smith III, and J. S. Abel, "Resolving wave digital filters with multiple/multiport nonlinearities," in *Proc. 18th Int. Conf. Digit. Audio Effects*, Trondheim, Norway, Nov. 30 – Dec. 3 2015, pp. 387–394.

[4] K. J. Werner, J. O. Smith III, and J. S. Abel, "Wave digital filter adaptors for arbitrary topologies and multiport linear elements," in *Proc. 18th Int. Conf. Digit. Audio Effects*, Trondheim, Norway, November 30 – December 3 2015, pp. 379–386.

[5] M. J. Olsen, K. J. Werner, and J. O. Smith III, "Resolving grouped nonlinearities in wave digital filters using iterative techniques," in *Proc. 19th Int. Conf. Digit. Audio Effects*, Brno, Czech Republic, Sept. 5–9 2016, pp. 279–286.

[6] D. T. Yeh, J. S. Abel, and J. O. Smith, "Automated physical modeling of nonlinear audio circuits for real-time audio effects—part I: Theoretical development," *IEEE Trans. Audio, Speech, Language Process.*, vol. 18, no. 4, pp. 728–737, 2010.

[7] M. Holters and U. Zölzer, "A generalized method for the derivation of non-linear state-space models from circuit schematics," in *Proc. 23rd European Signal Process. Conf.*, Nice, France, Aug. 31 – Sept. 4 2015, pp. 1073–1077.

[8] M. Holters and U. Zölzer, "A k-d tree based solution cache for the non-linear equation of circuit simulations," in *Proc. 24th European Signal Process. Conf.*, Budapest, Hungary, Aug. 29 – Sept. 2 2016, pp. 1028–1032.

[9] V. Duindam, A. Macchelli, S. Stramigioli, and H. Bruyninckx, *Modeling and Control of complex Physical Systems: The Port-Hamiltonian Approach*, Springer Berlin Heidelberg, 2009.

[10] D. Fränken, J. Ochs, and K. Ochs, "Generation of wave digital structures for networks containing multiport elements," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 3, pp. 586–596, Mar. 2005.

[11] T. Schwerdtfeger and A. Kummert, "A multidimensional signal processing approach to wave digital filters with topology-related delay-free loops," in *IEEE Int. Conf. Acoust., Speech, Signal Process.*, Florence, Italy, May 4–9 2014, pp. 389–393.

[12] S. Petrausch and R. Rabenstein, "Wave digital filters with multiple nonlinearities," in *Proc. 12th European Signal Process. Conf.*, Vienna, Austria, Sept. 6–10 2004, vol. 12, pp. 77–80.

[13] T. Schwerdtfeger and A. Kummert, "Newton's method for modularity-preserving multidimensional wave digital filters," in *IEEE 9th Int. Workshop Multidimensional (nD) Syst. (nDS)*, Vila Real, Portugal, Sept. 7–9 2015.

[14] R. C. D. Paiva, S. D'Angelo, J. Pakarinen, and V. Välimäki, "Emulation of operational amplifiers and diodes in audio distortion circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 10, pp. 688–692, Oct. 2012.

[15] D. T. Yeh and J. O. Smith, "Simulating guitar distortion circuits using wave digital and nonlinear state-space formulations," in *Proc. 11th Int. Conf. Digit. Audio Effects*, Espoo, Finland, Sept. 1–4 2008, pp. 19–26.

[16] K. J. Werner, V. Nangia, A. Bernardini, J. O. Smith III, and A. Sarti, "An improved and generalized diode clipper model for wave digital filters," in *Proc. 139 Int. Audio Eng. Soc.*, New York, NY, Oct. 29 – Nov. 1 2015.

[17] W. R. Dunkel, M. Rest, K. J. Werner, M. J. Olsen, and J. O. Smith III, "The Fender Bassman 5F6-A family of preamplifier circuits—a wave digital filter case study," in *Proc. 19th Int. Conf. Digit. Audio Effects*, Brno, Czech Republic, Sept. 5–9 2016, pp. 263–270.

[18] J. Pakarinen and M. Karjalainen, "Enhanced wave digital triode model for real-time tube amplifier emulation," *IEEE Trans. Audio, Speech, Language Process.*, vol. 18, no. 4, pp. 738–746, May 2010.

[19] M. Karjalainen and J. Pakarinen, "Wave digital simulation of a vacuum-tube amplifier," in *Proc. IEEE Int. Conf. Acoust., Speech, Signal Process.*, Toulouse, France, May 14–19 2006, vol. 5.

[20] S. D'Angelo, J. Pakarinen, and V. Välimäki, "New family of wave-digital triode models," *IEEE Trans. Audio, Speech, Language Process.*, vol. 21, no. 2, pp. 313–321, Feb. 2013.

[21] K. J. Werner, W. R. Dunkel, M. Rest, M. J. Olsen, and J. O. Smith III, "Wave digital filter modeling of circuits with operational amplifiers," in *Proc. 24th European Signal Process. Conf.*, Budapest, Hungary, Aug. 29 – Sept. 2 2016, pp. 1033–1037.

[22] T. Stilson and J. Smith, "Alias-free digital synthesis of classic analog waveforms," in *Proc. Int. Comput. Music Conf.*, Hong Kong, China, Aug. 19–24 1996, pp. 332–335.

[23] Eli Brandt, "Hard sync without aliasing," in *Proc. Int. Comput. Music Conf.*, Havana, Cuba, Sept. 17–23, 2001, pp. 365–368.

[24] Vesa Välimäki, Jussi Pekonen, and Juhan Nam, "Perceptually informed synthesis of bandlimited classical waveforms using integrated polynomial interpolation," *J. Acoust. Soc. America*, vol. 131, no. 1, pp. 974–986, 2012.

[25] F. Esqueda and V. Välimäki, "Rounding corners with BLAMP," in *Proc. 19th Int. Conf. Digit. Audio Effects*, Brno, Czech Republic, Sept. 5–9 2016, pp. 121–128.

[26] J. D. Parker, V. Zavalishin, and E. Le Bivic, "Reducing the aliasing of nonlinear waveshaping using continuous-time convolution," in *Proc. 19th Int. Conf. Digit. Audio Effects*, Brno, Czech Republic, Sept. 5–9 2016, pp. 137–144.

[27] S. Bilbao, F. Esqueda, J. D. Parker, and V. Välimäki, "Antiderivative antialiasing for memoryless nonlinearities," *IEEE Signal Process. Lett.*, 2017, to be published, DOI 10.1109/LSP.2017.2675541.

[28] Dietrich Fränken and Karlheinz Ochs, "Automatic step-size control in wave digital simulation using passive numerical integration methods," *AEU – Int. J. Electron. Commun.*, vol. 58, no. 6, pp. 391–401, 2004.

[29] K. J. Werner, M. J. Olsen, M. Rest, and J. D. Parker, "Generalizing root variable choice in wave digital filters with grouped nonlinearities," in *Proc. 20th Int. Conf. Digit. Audio Effects*, Edinburgh, U. K., Sept. 5–9 2017.

[30] Paul Horowitz and Winfield Hill, *The Art of Electronics*, Cambridge University Press, Cambridge, UK, second edition, 1980.

[31] Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, Oxford University Press, Inc., New York, NY, USA, 6th edition, 2009.

[32] R. L. Burden and D. J. Faires, *Numerical Analysis*, Brooks/Cole, Cengage Learning, Boston, MA, 9th edition, 2010.